Silicon Nanotechnology Challenges and Polymer Opportunities

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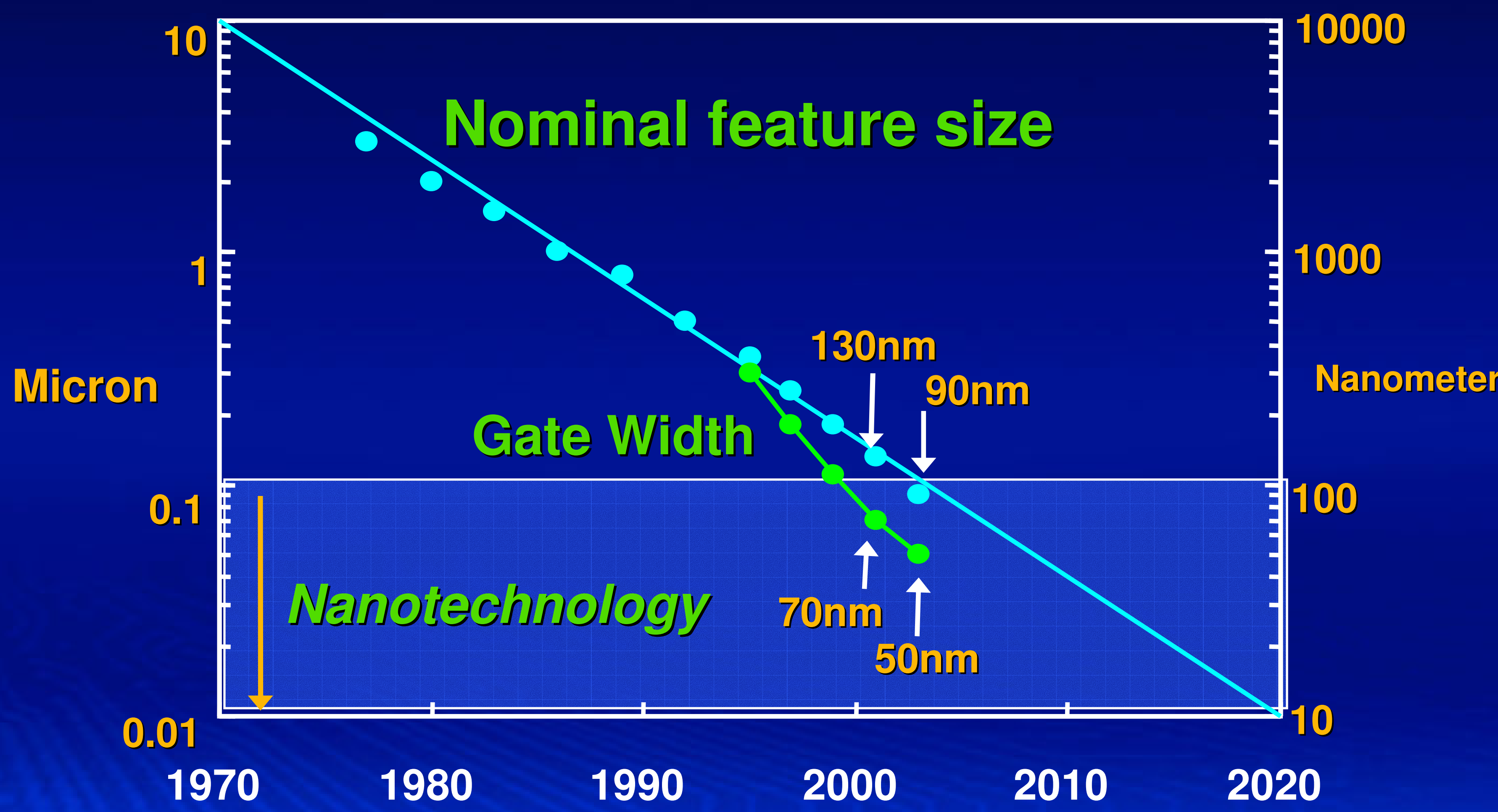
Agenda

- Technology Trends & Drivers
- Materials Challenges
  - ➔Silicon Nanotechnology
  - ➔High Integration packages
  - ➔High Performance Packages
  - ➔Laminate Substrates & Printed Wiring Boards
- Future Polymer Challenges and Nanotechnology
- Polymers by Design
- Summary

Key Messages

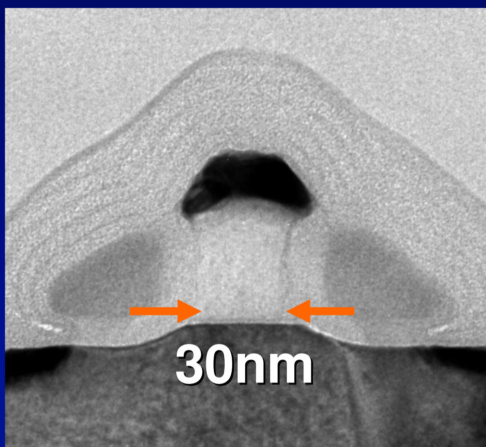
- New silicon technologies require improved polymers
- Silicon technology & market forces require new package technologies
- Stringent polymer performance requirements
  - → Application
  - → Process
  - → Use
- Polymers by Design….

Technology Scaling

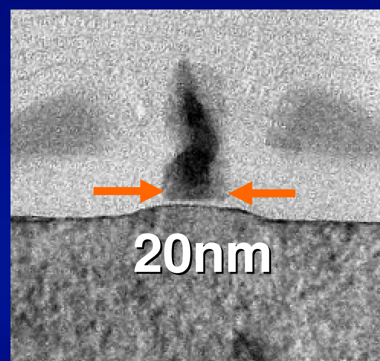


Intel's Transistor Research in Deep Nanotechnology Space

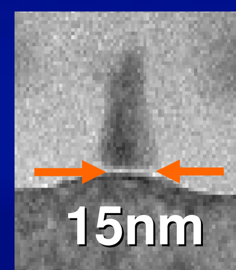
Experimental transistors for future process generations



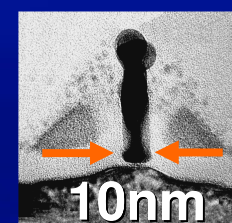
65nm process
2005 production



45nm process
2007 production



32nm process
2009 production

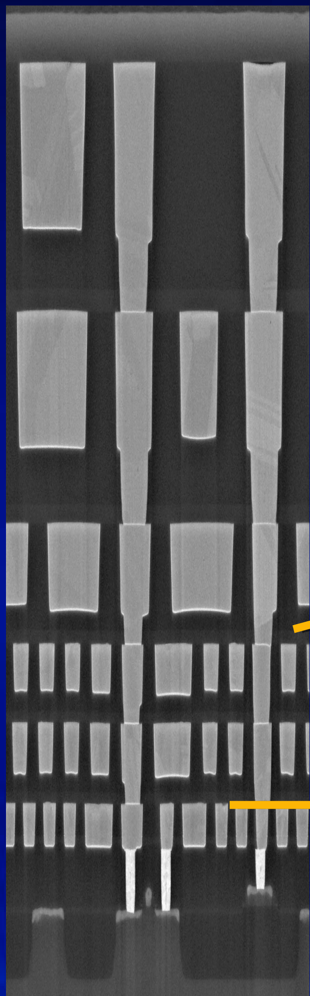


22nm process
2011 production

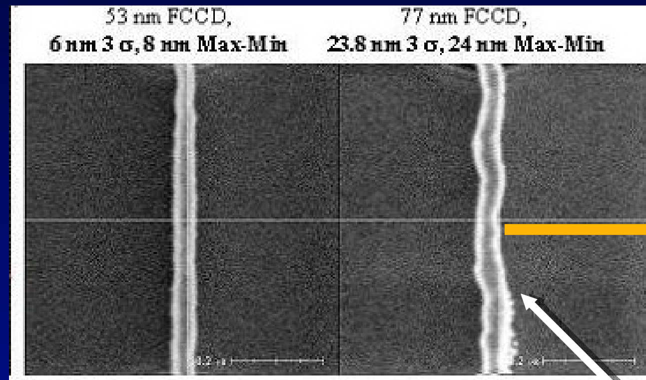
Transistors will be improved for production

Source: Intel

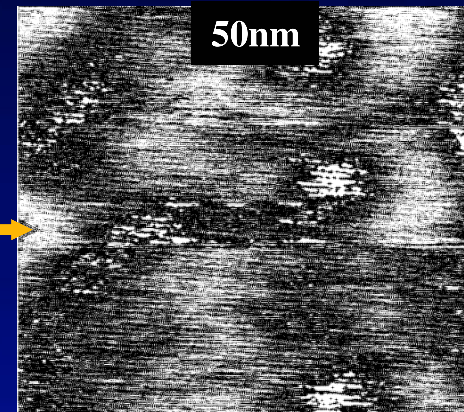
Material Challenges



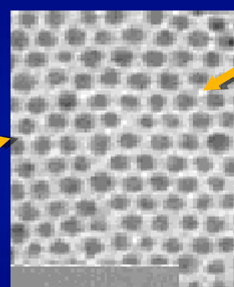
PPT Shrink
Source: Intel



Print Features Line Edge Roughness(LER)



Resist Nano-domains

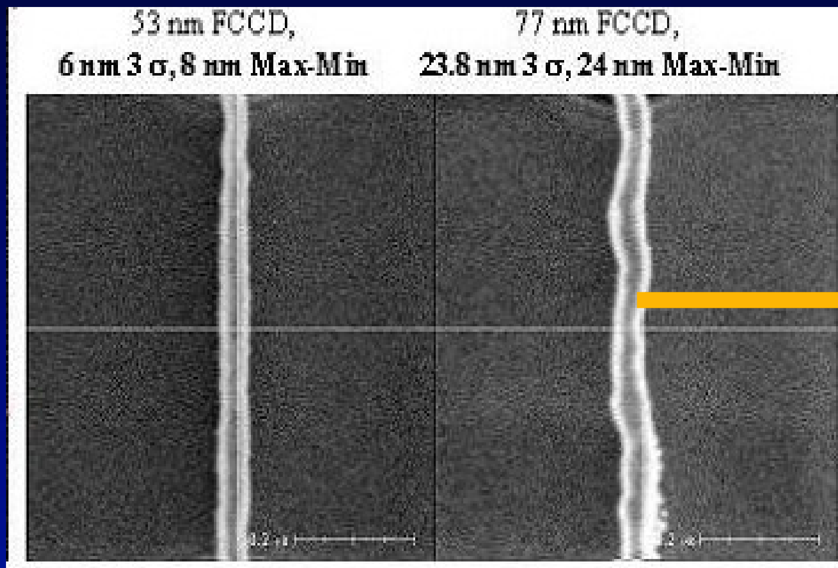


Low K Interlevel Dielectric
Micelle Assembled….

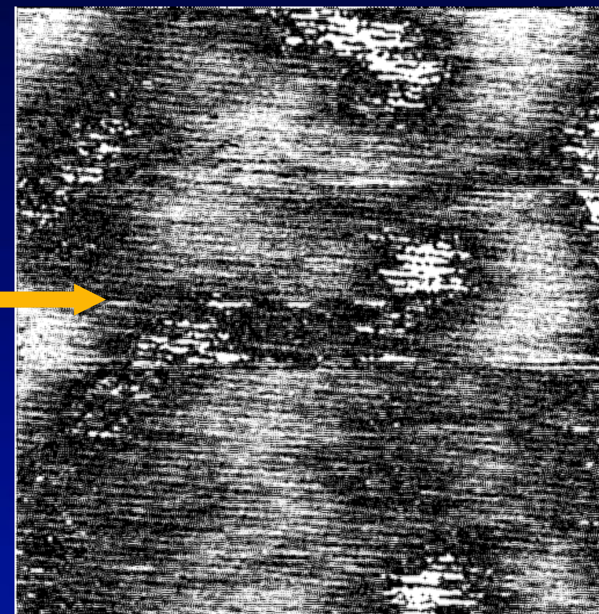
Planarized interconnects and ILD

Materials Challenges Everywhere

Future Lithography Resist Challenges



Line Edge Roughness(LER)

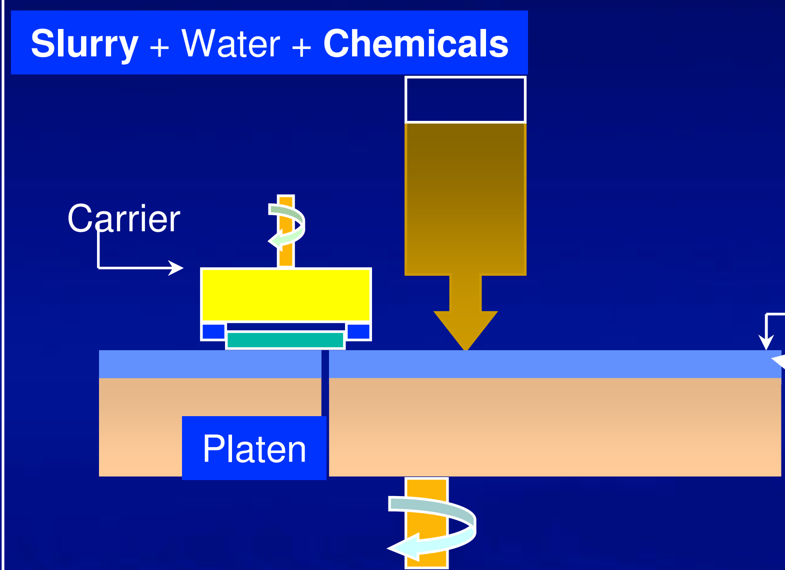


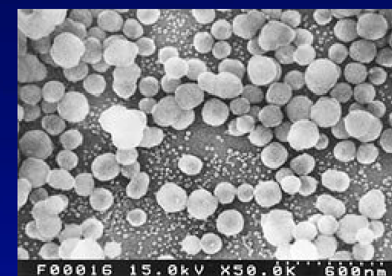
Atomic Force Microscope Picture of Resist Nano-domains (50nm X 50nm)

- Resist nano-domains limiting feature resolution and defects.
  - *Requires control at the molecular level*

Chemical Mechanical Polish

Chemical Mechanical Planarization (CMP)





100nm-200nm
Slurry Particles

- Tunable compressibility w/o affecting the removal rate
- Tunable surface hydophobicity independent of slurry and/or chemistry pH.
- Minimum wear rate as a result of conditioning
- Minimum or no break-in required

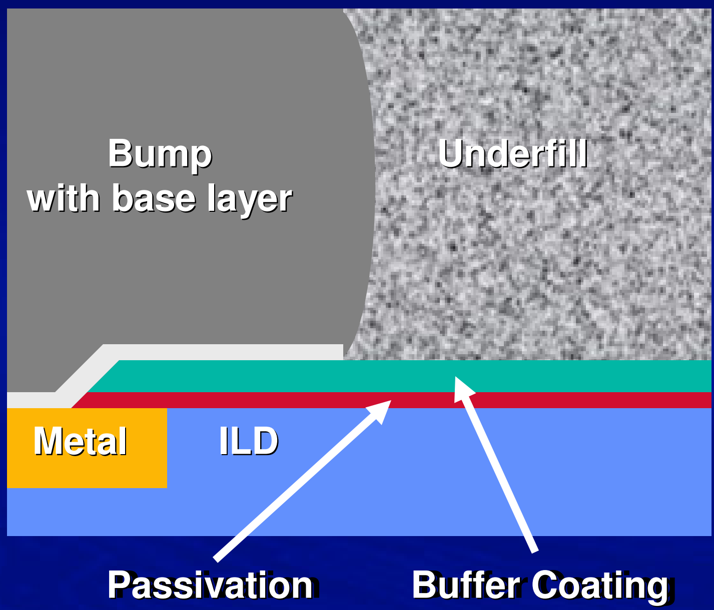
Improved performance & properties through the life of use
Improved pad life

•Electro-polish or Ultra Lower Pressure CMP for Nanoscale Features

Buffer Coating – Integrated Challenges

Buffer Coating Requirements

- Die-package CTE mismatch in flip-chip packages
- Increased processing temperatures for Pb-free

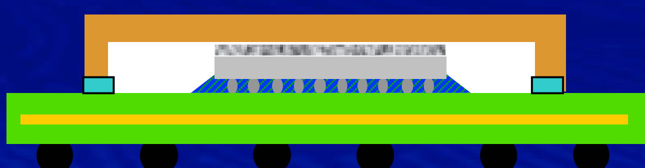


- Thermal / thermomechanical
  - Reduce cure temperature
  - Absorb increased package-induced stresses due to Pb-free processing temps
  - Reduce CTE
- Adhesion
  - Strong adhesion to underfill, bump , barrier layers, and passivation

Buffer coating challenges are becoming highly integrated!

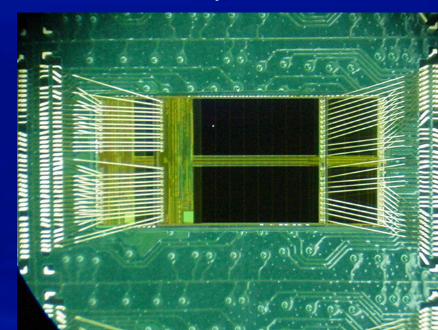
Product & Package Trends

Computing



High Performance Package

Converged Communication & Computing



High Integration Package

Market & Technology are driving new package solutions

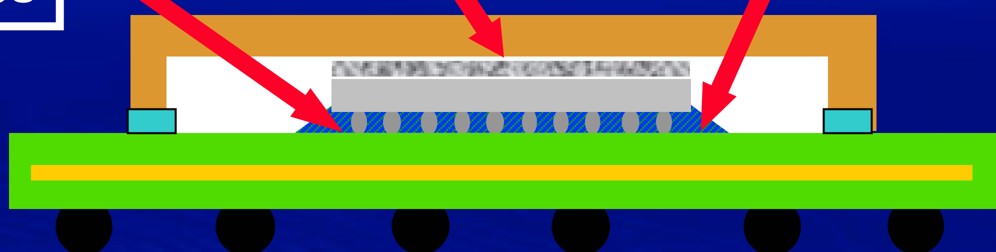
High Performance Package

High Performance Packages

Thermal Interface Material
Thermal Conductivity
Young's Modulus
Cure Temperature
Viscosity
Moisture Absorption

Flip Chip Trend:
Closer bump spacing
Shorter bumps

Underfill
CTE =CTE of FC Joint
Cure Temperature
Adhesion
Moisture absorption

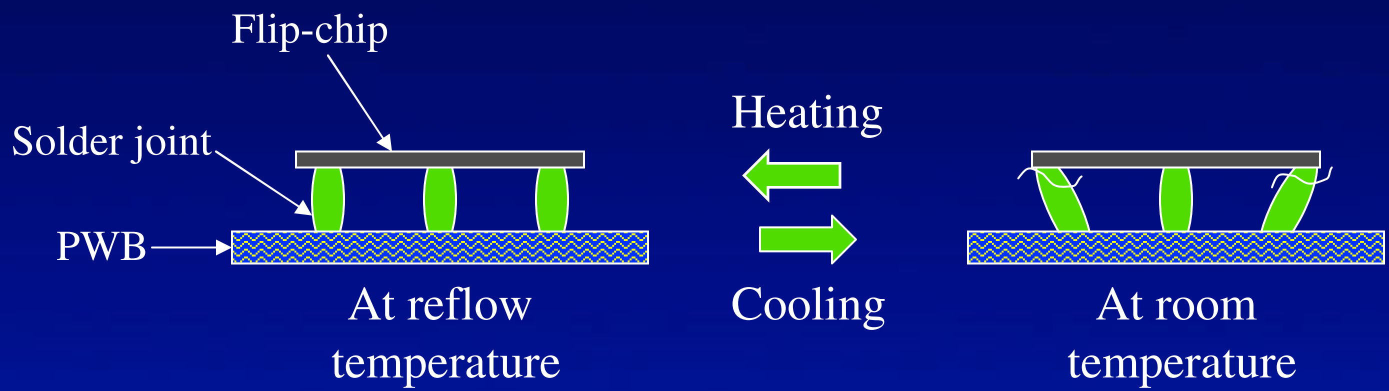


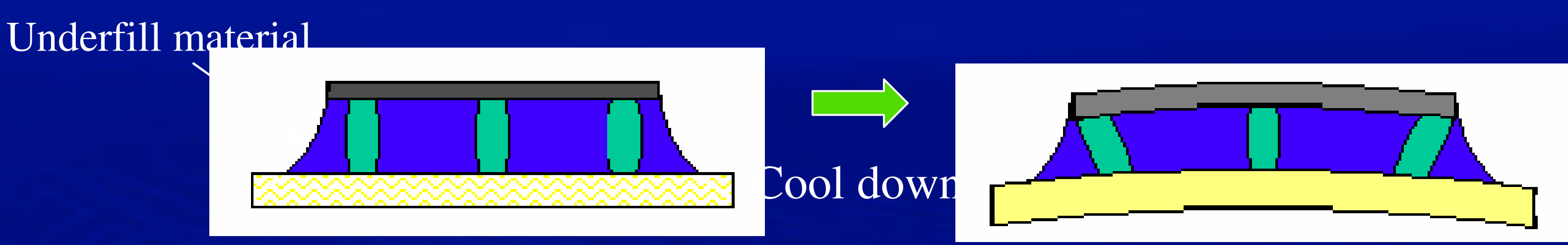
Substrate
CTE
Modulus
Adhesion
Tg
Dielectric constant
Loss factor

Properties must be optimized for application, process, and use

UF Overview - UF Mechanism

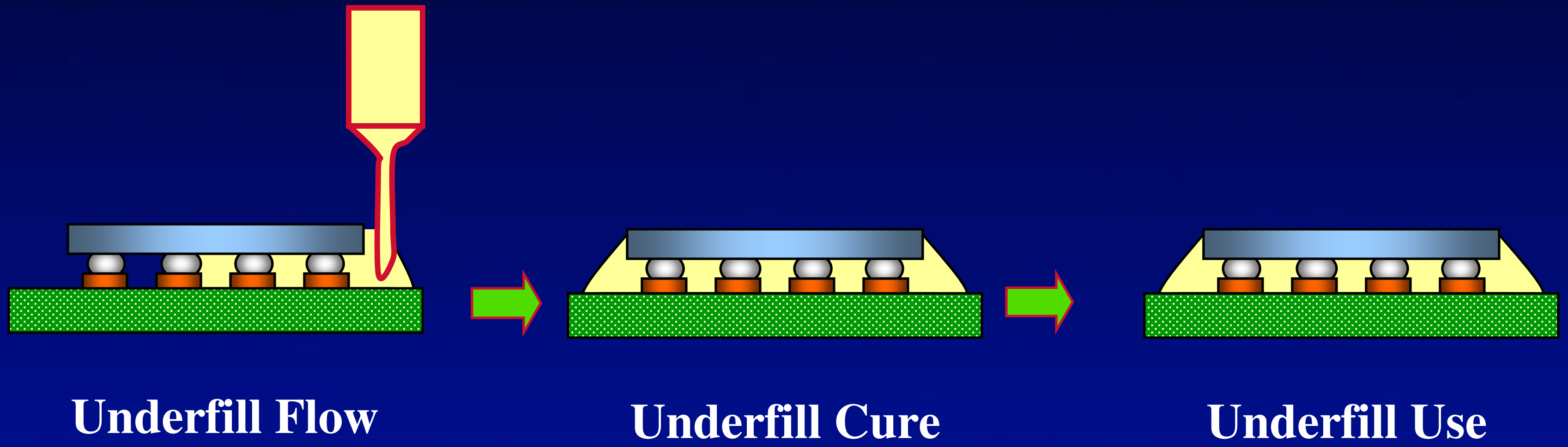
The mechanism of underfill protecting flip chip joint





- Substrate and chip are interlocked by underfill
- The strain on joint is converted to deformation
- Joint is compressed and protected by underfill

Capillary Flow Underfill

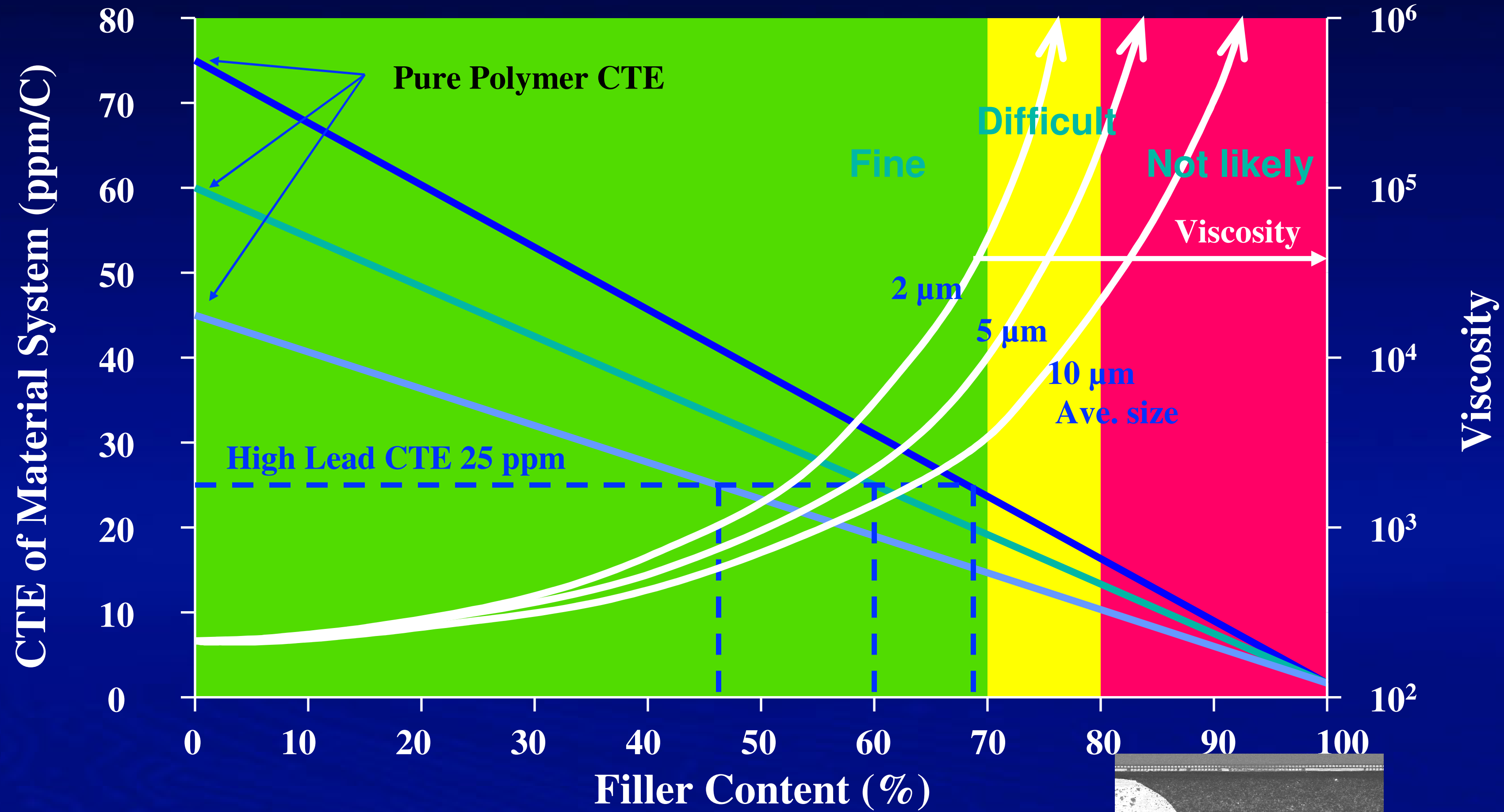


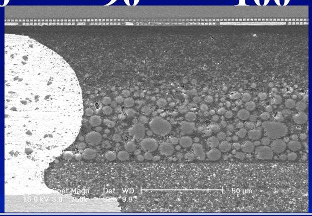
Application Properties
- Viscosity
- Wetting
- Uniformity of Filler Distribution

Process Properties
- CTE
- Wetting
- Young's Modulus
- Cure Temperature

Use Properties
- CTE (T)
- Tg
- Young's Modulus
- Adhesion
- Moisture Absorption
- Toughness
- 260C Board Assembly
- Temperature (-25 to 125C)

UF Material Requirement



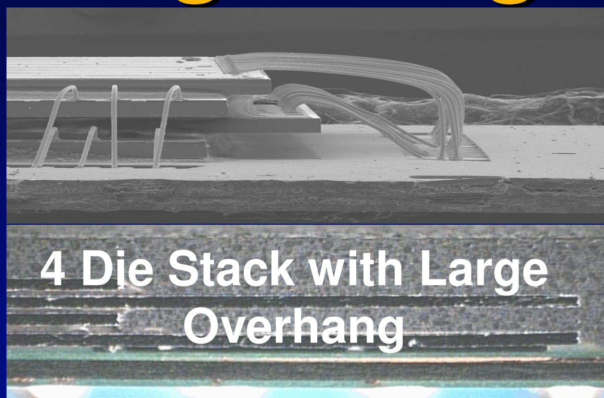


- Filler size must be reduced to improve uniformity

Need Low Viscosity – low CTE polymers

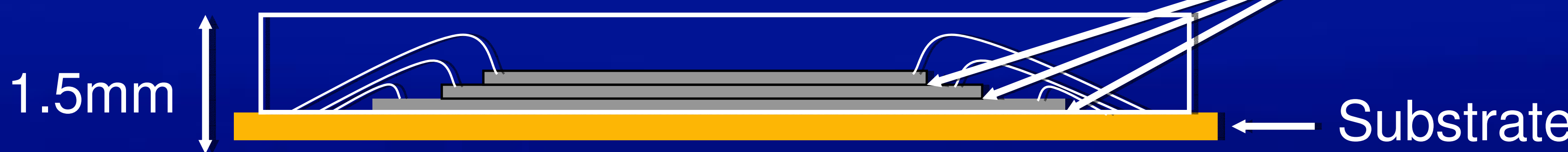
High Integration Packages

High Integration Packages


4 Die Stack with Large Overhang

Molding Compound
CTE
Local CTE
Future Thermal Conductivity
Low Stress

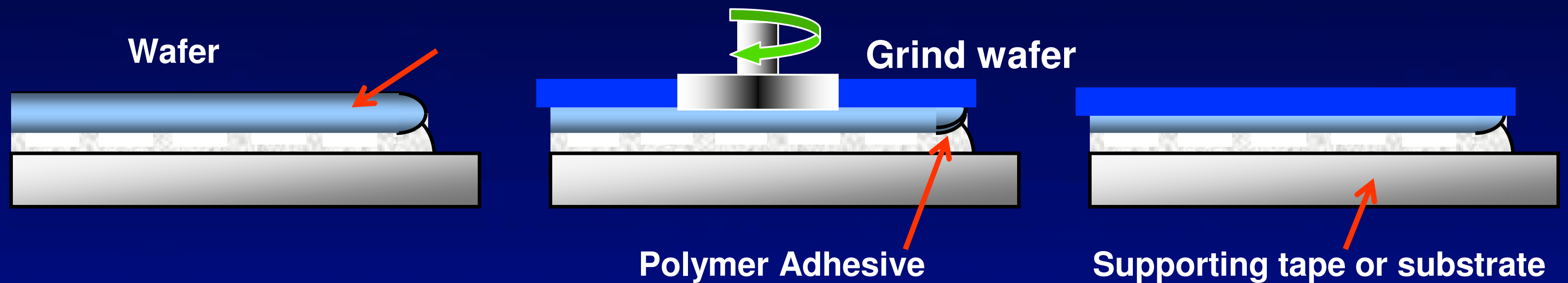
Die Attach Adhesive
Adhesion (Low T cure)
Shrinkage
Cure Temperature
Modulus
Tg
Moisture Absorption
Thickness



Technology Trends

- More chips per package ➡ Thinner chips, adhesive & substrate
- Lead Free ➡ All materials must be stable with 260C board assembly

Wafer Grinding Polymer Adhesive Challenge



Wafer Grinding Polymer Adhesive Challenge

Process ability
- Perfectly applied to wafer surface
- No void, no defect
- Minimum total thickness variation

Mechanical property
- Protect bump, wafer surface, and wafer edge
- Balanced modulus and toughness of adhesive
- Protect wafer from dimpling and chipping

Thermal property
- Minimum outgasing of adhesive
- Thermal stability >150ºC for most applications

Adhesive release ability
- Dry release, UV, thermal release or mechanical peeling (no solvent)
- Clean release, no or minimum residue without cleaning
- No wafer damage during adhesive releasing

High Integration Packages
Die Attach Adhesives

<u>Application Properties</u>
- Adhesion
- Thickness
- Modulus
- Defects

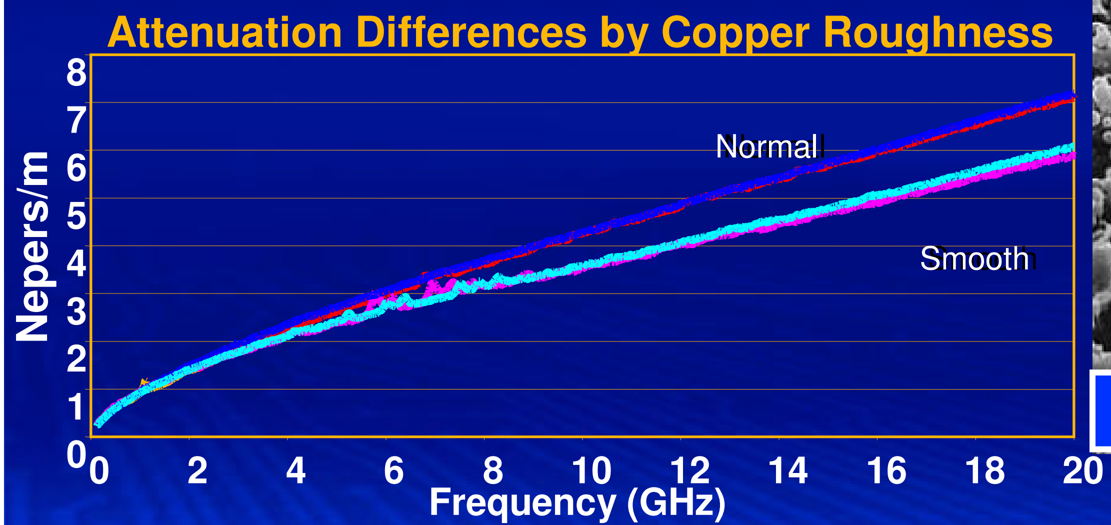
<u>Process Properties</u>
- Adhesion
- CTE
- Partial Cure Properties
- 160C Wire Bond
- Full Cure Temperature
- Mold Compound Cure
- Modulus

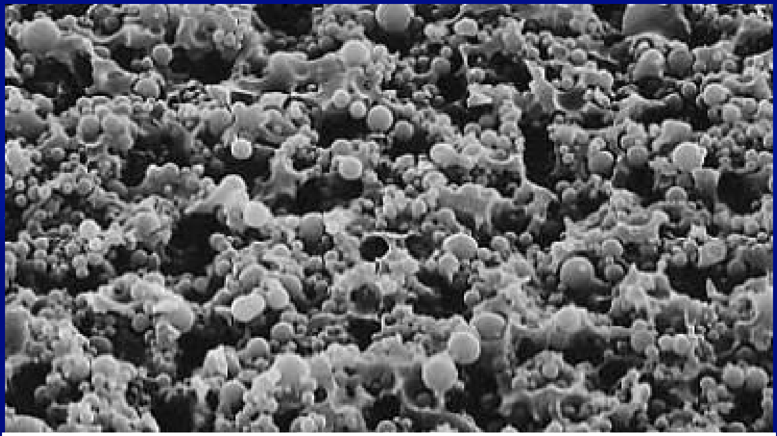
<u>Use Properties</u>
- Adhesion
- CTE
- 260C Board Assembly
- Modulus
- Moisture absorption
- Toughness

Laminate Substrates & Printed Wiring Boards

Polymer / Metal Adhesion

- **Drivers:**
  - ➔ Copper roughness increases skin effect loss
  - ➔ Electrical speeds require lower loss
- **Issues**
  - ➔ Adhesion over temperature
  - ➔ Surface Treatment Variations



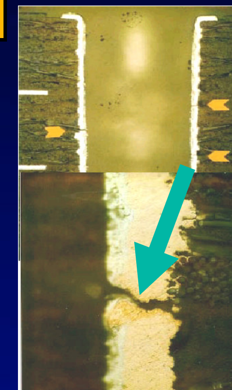


Surface roughened for electroplating

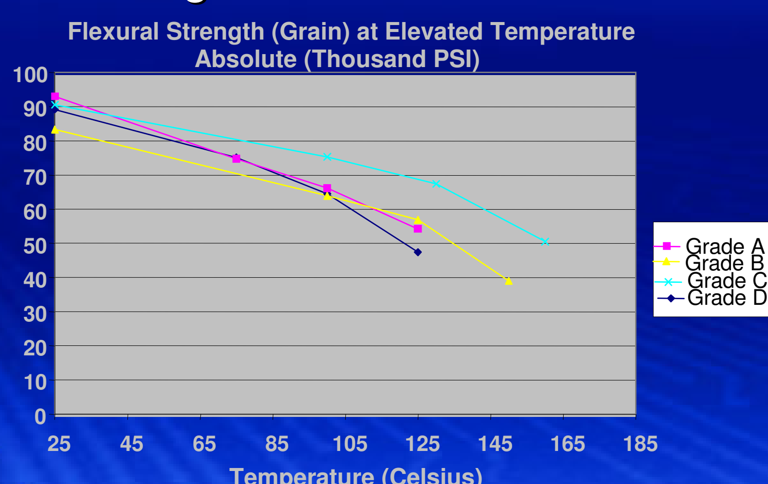
Improve adhesion with reduced roughness and without " lossy" coatings

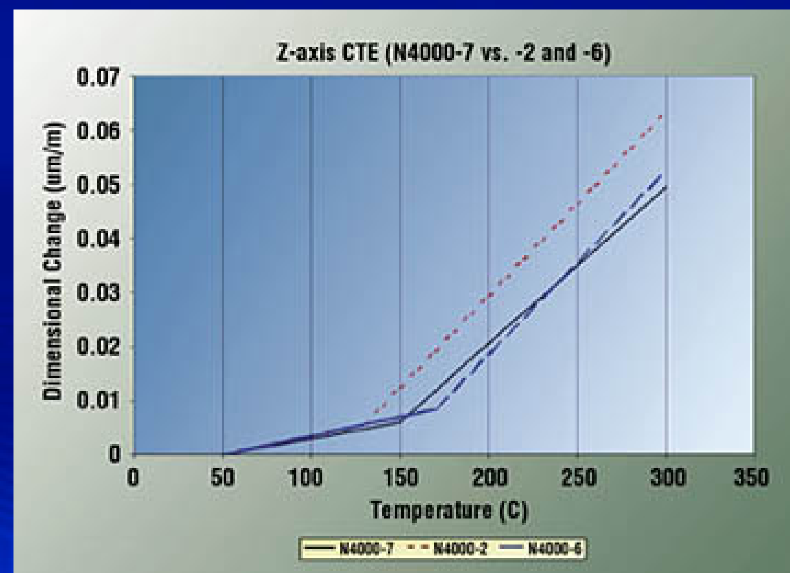
Processing & Use Thermal Mechanical Challenge

- Via Reliability Concerns
  - ➔ 260C Board Assembly (> 0.07” thick boards)
  - ➔ Max Operating Temps >130C
  - ➔ Thermal Cycle Stress
    - ⇨ Modulus vs Temperature
    - ⇨ CTE vs Temperature
    - ⇨ Adhesion vs Temperature
    - ⇨ Toughness



Interconnect:
Barrel
And
Post





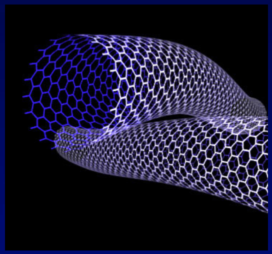
Challenges Summary

- Different Materials Properties needed
  - → Application
  - → Process
  - → Use
- Critical Properties
  - → CTE, Modulus, Cure Temperature, Tg, Adhesion, 260C stability
- Complex Property Requirements

Challenge: Polymers by Design

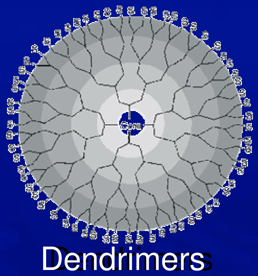
- Need Polymers to meet complex multi-property requirements
- Predictive models for polymer properties
  - → Application, process, and use
- New building blocks with characterized properties
- New characterization metrology and methodologies

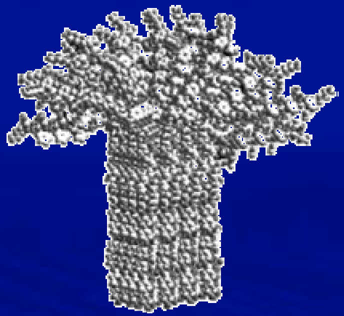
Nanotechnology Elements



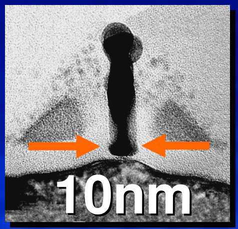
Sub 100nm particles

c.
olecular Assembly (directed and self assembly)





Macromolecules



Sub 100nm structures

Role for Macromolecules, self assembly and nanoparticles?

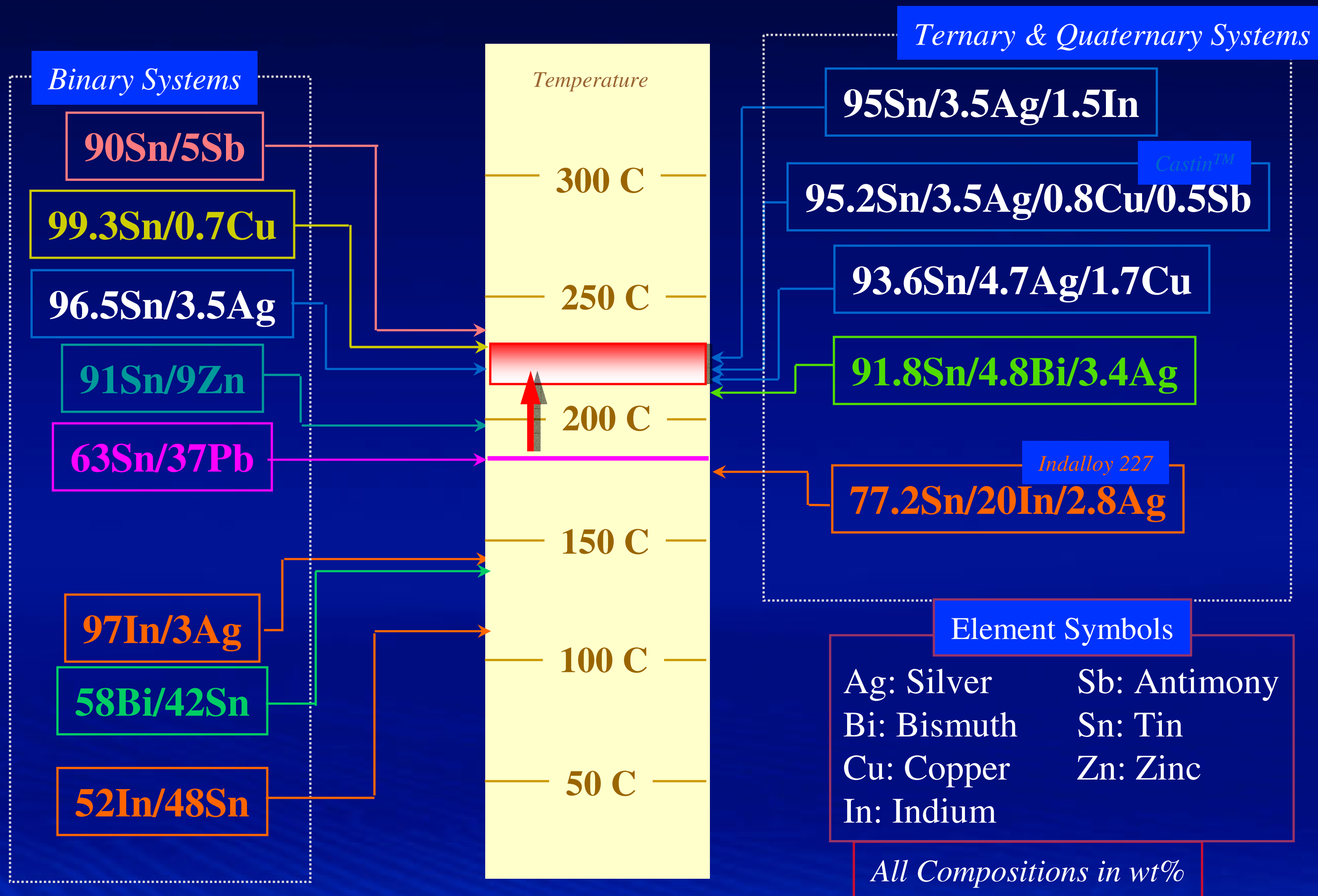
Summary

- Silicon Nanotechnology is creating significant polymer challenges
- Future polymers must deliver multiple complex properties
  - ➔Application, process, and use
- Need Polymers by design
  - ➔Predictive properties
  - ➔Characterized building blocks
  - ➔Models for material performance

For further information on Intel's silicon technology and Moore’s Law, please visit the Silicon Showcase at www.intel.com/research/silicon

Back-up

Lead Free Transition



- **Lead Free Solders require higher assembly temperatures**